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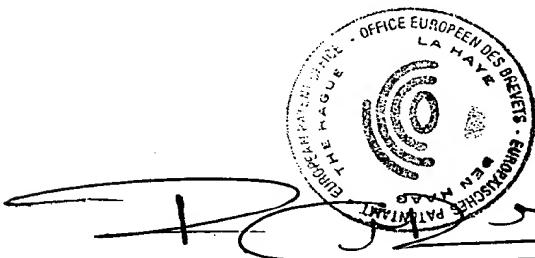
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Patentanmeldung Nr. Patent application No. Demande de brevet n°

00403506.9



R.C. VAN DIJK

Der Präsident des Europäischen Patentamts;
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Sheet 2 of the certificate
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1 MULTIPLE INPUT, MULTIPLE OUTPUT CHANNEL,2 DIGITAL RECEIVER TUNER

3

4 Inventor: Fabien Buda

5

6 BACKGROUND

7

8 Hybrid Fiber Coax (HFC) networks have been used for some time to implement or
9 upgrade metropolitan area cable television systems. In a recent improvement to HFC
10 networks, mini-Fiber-Nodes (mFNs) have been employed to extend fiber closer to
11 subscribers, each mFN providing bidirectional fiber-based services (including Internet
12 access via cable modem) for multiple-tens of subscribers. mFNs are intended to be
13 compact units deployed in the field, generally in aerial-wire or utility-pole-mount
14 configurations, and include at least one "upstream" receiver. An upstream receiver is
15 a receiver in the return direction, that is, in the direction from the subscriber to the
16 cable head end. Generally multiple coaxial (coax) cables, each carrying upstream
17 signals corresponding to a different group of subscribers, may terminate at the mFN
18 for subsequent upstream transmission via fiber.

19

20 Each of these coax cables generally has a wide spectrum (up to 1GHz) including a
21 multiplex of upstream carriers located in the 5-42 MHz range. In accordance with the
22 DOCSIS industry standard, each upstream carrier may have any symbol rate from 5
23 possible values (160 kBaud, 320 kBaud, 640 kBaud, 1280 kBaud, 2560 kBaud) with a
24 modulation format of either QPSK or 16-QAM. In addition, each upstream carrier
25 has a power spectrum density variation, with respect to a nominal value, of ± 6 dB. In
26 a worst-case scenario for the upstream receiver, the 5-42MHz band may be filled with

1 (up to 11) undesired carriers operating with the maximum baud rate (2560 kBaud) and
2 a desired carrier may have the smallest value 160 kBaud. Furthermore, there may be
3 up to a 12 dB difference in power spectrum density between the desired carrier and
4 the others.

5

6 A digital receiver may be partitioned into a tuner and digital demodulator portions.
7 The tuner accepts one or more broadband analog inputs having a variety of desired
8 and undesired signals. The tuner's purpose is to isolate the desired signals and
9 provide baseband-translated digitized equivalents for subsequent processing in the
10 demodulator. Because quadrature modulation is common, the outputs are often
11 provided in quadrature. The stage(s) where frequency translation is performed is (are)
12 generally referred to as the receiver front-end. The stages where digitization is
13 performed may be referred to as the A/D (ADC, analog to digital converter, or
14 digitizer). The stages before and after the A/D are necessarily analog and digital,
15 respectively.

16

17 A traditional tuner for an upstream digital receiver is shown in Fig. 1. A first IF
18 (intermediate frequency) conversion combined with a SAW (surface acoustic wave)
19 filter is used for isolating the desired carrier and suppressing any and all undesired
20 carriers. Next, down-conversion is done in the analog domain by in-phase splitting the
21 isolated carrier and mixing with 2 analog LOs (local oscillators). The analog LOs are
22 provided in quadrature at the expected channel spacing. Each of the resulting
23 quadrature signals from the mixers is then coarse anti-alias filtered in the analog
24 domain and sampled with respective A/Ds. Matched filtering after the A/Ds is
25 subsequently performed in the digital domain. The quadrature output signal pair of the
26 matched filter may then be provided to the demodulator of the desired carrier/channel.

1 There are a number of significant costs associated with each required stage of any
2 digital receiver tuner. Costs are minimized by keeping stages as simple as possible
3 and as few in number as necessary. Another stage cost is associated with the bit-
4 width of the digital stages. Each additional bit in width incrementally increases the
5 cost, size, and complexity of the associated receiver. Since the dynamic range of the
6 signals being processed necessitates a proportional bit-width, the dynamic range
7 should be minimized consistent with maintaining good performance. Because A/Ds
8 are often the most complex and expensive sub-systems in the tuner, the number of
9 required A/Ds is a key implementation consideration. In addition, each A/D has an
10 associated clock sub-system (not shown in Fig. 1 but known to practitioners of the art)
11 that must be configured appropriately for the carrier being digitized. The number and
12 extent of required clock sub-systems is thus also an important implementation
13 consideration.

14

15 Traditional digital receiver approaches have required the entirety of the above-
16 described tuner per desired carrier/channel. In the mFN augmented HFC systems
17 discussed above, because of the associated expense, bulk, and complexity of the
18 traditional tuners, it has not been considered practical in widespread deployment to
19 demodulate upstream signals locally at the mFN. Accordingly, the entire spectrum of
20 each coax has been indiscriminately sent upstream over fiber via either analog or
21 digital techniques for remote reconstruction and demodulation at the cable head end
22 (or intermediate upstream location). Accordingly, when multiple coaxial cables
23 terminate into the mFN, either multiple expensive fibers are required or expensive
24 WDM techniques have been used to multiplex the multiple coax spectra onto
25 respective "lambda" wavelengths of a single fiber. In these approaches, the ultimately

1 demodulated upstream information content is a small fraction of the transmitted
2 upstream bandwidth.

3

4 In applications (such as upstream cable modem traffic) where there are multiple
5 desired channels on each of generally multiple input coaxial cables, the use of
6 traditional digital receivers (requiring one tuner per desired carrier/channel) results in
7 a confusing proliferation of associated splitters, connectors, and couplers.

8 Provisioning (establishing the operating configuration of) a particular upstream
9 subscriber signal (out of many) over a particular upstream channel (again out of
10 many) generally necessitates error-prone manual configuration of multiple coaxial
11 cables, splitters, connectors, and couplers. This hardware also introduces new noise
12 and signal losses. Provisioning additionally involves configuration of the receiver to
13 accommodate the carrier frequency and baud-rate of the transmitted signal. To
14 change the carrier frequency dynamically in the traditional digital receiver requires a
15 very agile and very costly local oscillator. Less expensive, less agile, local oscillators
16 generally necessitate error-prone manual configuration of component modules or
17 component settings.

18

19 It is thus seen that there are many shortcomings to the traditional tuner approaches to
20 multiple input, multiple output channel, digital receivers. What is needed is an
21 optimized tuner for such receivers that is efficient, cost sensitive, flexible, and
22 minimizes noise and signal loss. What is needed is a multiple input, multiple output
23 channel, digital receiver tuner that reduces the number of signal processing stages, the
24 stage bit-widths, the number of A/Ds, and the number and extent of clock sub-systems
25 compared with traditional approaches. What is further needed is a compact and
26 efficient multiple input, multiple output channel, digital receiver that performs local

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- 1 demodulation and is suitable for widespread field deployment in distributed communication systems and networks.
- 2

3

4

5

1

SUMMARY

2

3 The present invention teaches a compact and highly integrated multiple-channel
4 digital tuner and receiver architecture, suitable for widespread field deployment,
5 wherein each receiver demodulator channel may be remotely, automatically,
6 dynamically, and economically configured for a particular cable, carrier frequency,
7 and signaling baud-rate, from an option universe that includes a plurality of input
8 cables, a plurality of carrier frequencies, and a plurality of available baud-rates. The
9 invention thus provides substantial additional flexibility and cost savings over
10 conventional multiple-channel receiver approaches where equivalent configuration
11 capability would require prohibitively expensive specialized components or costly
12 manual operations that cannot be implemented automatically. Tuners and digital
13 receivers implemented in accordance with the present invention also minimize the
14 number of required A/Ds, number and extent of clock sub-systems, bit-width of
15 digital processing stages, and overall complexity. The architecture has broad generic
16 applicability, but offers particular advantages in multiple (coax) input, multiple
17 channel output, digital receivers. In a series of illustrative embodiments, the
18 teachings of the invention are applied to an upstream digital receiver sub-system for
19 use in the mFNs of an HFC network.

20

21 In accordance with a first aspect of the present invention, an illustrated multiple coax
22 input, multiple channel output, digital tuner embodiment is partitioned into a multiple
23 coax input digitizer portion and a multiple channel output front-end portion. The
24 digitizer portion consists of a number (N) of digitizers and accepts input signals from
25 N coax cables and digitizes them with respective A/D (Analog-to-Digital) converters.
26 This creates N streams of digitized input data, respectively corresponding to each

1 coax cable. The front-end portion consists an independent number (M) of front-ends
2 and provides M channel outputs, which are streams of baseband-translated digital
3 words suitable for subsequent processing by M respective demodulators. At the input
4 to each of the M front-ends is a respective input selector coupled to each of the N
5 streams of digitized input data. Thus, each of the M front-ends is selectively
6 configurable to process digitized input data corresponding to any of the N coax
7 cables. Collectively, the input selectors comprise a selector bank. The selector bank
8 is a compact and efficient implementation that elegantly operates in the digital
9 domain to provide functionality previously performed in the analog domain by bulky
10 analog splitters that are problematic and costly to provision.

11

12 In accordance with a second aspect of the present invention, a variable-gain amplifier
13 is situated before the A/D converter used to digitize the input signals for each of the N
14 coax inputs, and a digital signal scaler is situated at the input of each of the M front-
15 ends. The variable-gain amplifier that precedes the A/D converter operates on the
16 entire carrier multiplex that is present on the associated coax. The amplifier gain is
17 set as a function of the entire carrier multiplex present on the coax and not by any
18 particular carrier. Each digital signal scaler is dedicated to a respective front-end
19 channel and therefore has a particular respective carrier of interest. The scaler
20 dynamically scales (shifts right or left by one or more bits) the incoming stream of
21 digitized input data as a function of the signal power of the respective carrier in order
22 to minimize variations in the peak magnitude of the signals processed. The scaler
23 thus manages the dynamic range such that the digital-word bit-width of the digital
24 front-end and subsequent demodulator stages can be minimized consistent with good
25 performance, substantially reducing the complexity and cost of the digital receiver.

26

1 In accordance with a third aspect of the present invention, a particular clocking
2 combination is used within the digital receiver tuner. A fixed predetermined A/D
3 sampling rate is chosen to provide oversampling of the inputs by a common integer
4 multiple of all the symbol rates of interest. Each oversampled input stream is digitally
5 down-converted to baseband and processed in three sample-frequency domains. The
6 first domain includes in common the A/Ds of the N digitizers, the baseband
7 converters and first decimators of the M front-ends, and operates at the fixed A/D
8 sample rate. In an optional but preferred embodiment, a second domain, including a
9 second decimator, operates at a fixed sub-multiple of the first domain. Additional
10 clock domains exist, including a plurality operating at selectable sub-multiples of the
11 first domain (or second domain, if any) as required to deliver a constant number of
12 symbol samples to each matched filter of the respective front-ends. This clocking
13 approach enables producing matched front-end outputs using only simple filters and
14 decimation, eliminates the need for interpolation stages, maximizes commonality of
15 function, and provides reduced complexity and costs over previous approaches.

16

1

Brief Description of Drawings

2

3 Fig. 1 illustrates a prior art tuner for a digital receiver.

4

5 Fig. 2 illustrates a tuner 1000 for a digital receiver in accordance with the present
6 invention, including a multiple-coax digitizer 900 and a multiple-channel front-end
7 6000.

8

9 Fig. 3 is a drawing providing additional detail of the splitting 2100 and selecting 2200
10 function blocks of the tuner 1000 of Fig. 2.

11

12 Figs. 4A-4D are drawings providing conceptual detail of the scaler 3000 of the tuner
13 1000 of Fig. 2 for four different operating cases. Fig. 4A illustrates the unity gain,
14 no-shift case. Fig. 4B illustrates a shift by one bit in the LSB direction. Fig. 4C
15 illustrates a shift by two bits in the LSB direction. Fig. 4D illustrates a shift by three
16 bits in the LSB direction.

17

18 Fig. 5 illustrates the baseband conversion 4000 and filtering and decimation 5000
19 function blocks of a single channel in the tuner 1000 of Fig. 2.

20

21 Fig. 6 illustrates preferred chip-boundary partitions for two different illustrative
22 embodiments of the tuner 1000 of Fig. 2

23

24 Figs. 7 and 8A-C illustrate exemplary system-level application of the present
25 invention. Fig. 7 illustrates a mini-Fiber-Node/mini-Cable-Modem-Termination-
26 System (mFN/mini-CMTS) 8000 using a DSP multiple-channel transceiver ASIC

1 7000, which implements in silicon the multiple-channel receiver front-end 6000
2 portion of the tuner 1000 of Fig. 2.
3
4 Figs. 8A-C illustrate the routing between a Head End 10100, the Internet 10000, and
5 Customer Premise Equipment (CPE) 8B, in a cable system architecture using the
6 mFN/mini-CMTS 8000 of Fig. 7. Fig. 8A provides particular detail of the routing
7 between the Head End 10100, Regional Packet Network 10150, mFN/mini-CMTS
8 8000, and CPE 8B. Fig. 8B provides particular detail of the CPE 8B. Fig. 8C
9 provides particular detail of the routing between the Head End 10100 and the Internet
10 10000.

11

12 Detailed Description

13

14 Fig. 2 illustrates a multiple coax input, multiple channel output, digital tuner 1000 for
15 a digital receiver in accordance with the present invention, including a multiple-coax
16 digitizer portion 900 and a multiple-channel front-end portion 6000. The digitizer
17 portion 900 consists of N Per-coax Digitizers 900-1 through 900-N, accepts input
18 signals 1800-1 through 1800-N from N coax cables, digitizes them with respective
19 A/D converters 930-1 through 930-N, and delivers to the front-end digitized signals
20 1700-1 through 1700-N. A Butterworth filter 910 and variable-gain amplifier 920
21 precedes each A/D converter. While a Butterworth characteristic is used in the
22 illustrative embodiment, this choice is not critical and other low-pass filters may also
23 be used. The variable-gain amplifier 920 is set by control 950 as a function of the
24 entire carrier multiplex present on the amplifier's associated coax input.
25 The front-end portion 6000 consists of M Per-channel Receiver Front-ends 6000-1
26 through 6000-M. The functions performed by front-end 6000 include splitting 2100,

1 selecting 2200, scaling 3000, baseband conversion 4000, and filtering and decimation
2 5000. Front-end 6000 provides M channel output quadrature pairs 1900-I1 through
3 1900-IM and 1900-Q1 through 1900-QM suitable for subsequent processing by M
4 respective digital demodulators. Digitized signals 1700-1 through 1700-N are
5 distributed to the individual selectors via splitting 2100. In accordance with control
6 2500, each selector 2000 couples a selected one of the digitized inputs to the
7 subsequent stages of the front-end. In accordance with control 3500, the digital signal
8 scaler 3000 dynamically scales the selected incoming stream as a function of the
9 signal power of the channel's associated carrier.

10

11 Clock domain 1100 includes in common the A/Ds 930-1 through 930-N of the N
12 digitizers 900-1 through 900-N and a first sub-portion of the M front-ends, and
13 operates at a fixed A/D sample rate chosen in accordance with a specific criteria to be
14 discussed below. A second clock domain 1200, including a second sub-portion of
15 the M front-ends, facilitates implementation and operates at a fixed sub-multiple of
16 the first domain. Additional clock domains exist, including a plurality 1300-1
17 through 1300-M operating at selectable sub-multiples of the first domain as required
18 to deliver a constant number of symbol samples to outputs of the front-end.

19

20 Digital Splitter

21 Fig. 3 is a drawing providing additional detail of the splitting 2100 and selecting 2200
22 function blocks of the tuner 1000 of Fig. 2. Digitized signals 1700-1 through 1700-N
23 are distributed to the individual selectors via splitting 2100, shown here as simple
24 distribution interconnect. Practitioners will understand that additional well-known
25 considerations such as buffering and attention to interconnect impedances and
26 parasitics may be required based on implementation specifics. In accordance with

1 control 2500, each selector 2000 couples a selected one of the digitized inputs to the
2 subsequent stages of the front-end. Practitioners will understand that the selectors
3 may use either encoded or uncoded controls and that the number of control bits will
4 vary based on this choice and the number of inputs being selected. The outputs 2250-
5 1 through 2250-M are provided to subsequent stages of the front-end.

6

7 Collectively, the input selectors comprise a selector bank. Via the selector bank, each
8 demodulator channel is selectively configurable to process digitized input data
9 corresponding to any of the coax cables. The selector bank elegantly operates in the
10 digital domain to provide functionality previously performed in the analog domain by
11 manual configuration of splitters, couplers, cables, and connectors that are
12 problematic and costly to provision.

13

14 Thus in accordance with the present invention, a modulated input signal
15 corresponding to a particular subscriber, and on a particular one of the coaxial cables,
16 can be routed (sent) to any particular one of the plurality of demodulator channels. In
17 the illustrative embodiment, the routing configuration is established during
18 provisioning of the upstream channel for each subscriber, the input selector for each
19 demodulator channel being controlled by digital commands transmitted from the head
20 end. Provisioning the upstream channel in this way reduces or eliminates the manual
21 configuration of connectors and couplers; reduces additional sources of noise and
22 signal losses; speeds setup; reduces costs; and increases flexibility. More generally,
23 the input selectors could be reconfigured dynamically, in response to predefined
24 criteria, to provide fault tolerance or minimization of transient interference.

25

1 Dynamic Range And Signal Power Management

2 The inventors discovered that control over signal power in digital receiver front-ends
3 is optimally managed through a cooperative combination of variable-gain amplifiers
4 in the analog domain and digital signal scalers in the digital domain. More
5 specifically, a variable-gain amplifier is situated before the A/D converter used to
6 digitize the input signals for each coax, and a digital signal scaler is situated at the
7 input of each front-end. (In accordance with the discussion above, the scaler is placed
8 after any selector function).

9

10 The variable-gain amplifier that precedes the A/D converter operates on the entire
11 carrier multiplex that is present on the associated coax. Recall that the output of the
12 A/D converter may be supplied to multiple demodulator channels, each typically
13 having a respectively unique carrier of interest. The gain of this amplifier is
14 considered appropriately set when the adjusted input to the A/D is such that the
15 digitized output generally spans the dynamic range of the A/D without significant
16 saturation. The amplifier gain is thereby set as a function of the entire carrier
17 multiplex present on the coax and not by any particular carrier. In a particular
18 illustrative embodiment the A/D provides a 12-bit 2's complement output. There is
19 only 11-bits of usable precision however, and the original LSB from the A/D is
20 ignored. The front-end subsequently operates on 11-bit 2's complement digital
21 words.

22

23 In an illustrative tuner embodiment compatible with the DOCSIS industry standard,
24 the power spectral density has a dynamic range of 12 dB. The modulated carrier
25 bandwidth dynamic range, which is proportional to a maximum-to-minimum symbol
26 rate ratio of 16, also is 12 dB. Since the product of the power spectral density and the

1 bandwidth gives received signal power for a selected carrier, the received signal
2 power has a 24 dB dynamic range for a selected carrier in this application. Thus, a
3 front-end designed for this application should have 24dB of headroom.

4

5 Unlike traditional approaches, the 24 dB of required dynamic range headroom is
6 accomplished through use of the digital scaler in accordance with the present
7 invention, and without additional bits over that required by the minimum signal case.
8 More specifically, the digital signal scaler reduces the complexity and the cost of the
9 front-end by limiting the dynamic range to the minimum necessary, while providing
10 good performance.

11

12 Each digital signal scaler is dedicated to a respective front-end channel and therefore
13 has a particular respective carrier of interest. The scaler dynamically scales the
14 incoming stream of digitized input data (by selective shift toward the LSB of zero to
15 three bits) as a function of the received nominal signal power of the respective carrier.
16 The scaler is operated to maintain essentially the same peak signal magnitude (having
17 3-dB of headroom) at the input to the next stage of the rest of the front-end (the
18 broadband conversion in the illustrative embodiment). As signals increase in
19 amplitude, the scaler selectively shifts by a proportionally greater numbers of bits,
20 providing increasing attenuation.

21

22 Figs. 4A through 4D are conceptual drawings of various shift configurations selected
23 by control 3500. In a preferred embodiment, the scaler is implemented using AND-
24 OR gating, but practitioners will understand that such shifting functions may be
25 readily implemented via a variety of other techniques. Fig. 4A illustrates the unity
26 gain, no-shift case, corresponding to small amplitude signals. Fig. 4B illustrates a

1 shift by one bit in the LSB direction, corresponding to division by 2 (attenuation to $\frac{1}{2}$
2 of the input magnitude). Fig. 4C illustrates a shift by two bits in the LSB direction,
3 corresponding to division by 4 (attenuation to $\frac{1}{4}$ of the input magnitude). Fig. 4D
4 illustrates a shift by three bits in the LSB direction, corresponding to a division by 8
5 (attenuation to $\frac{1}{8}$ of the input magnitude).

6

7

8 Front-End Stages

9 Within the previously discussed digitizer portion of the tuner 1000 of Fig. 2, the
10 received signal is oversampled by an A/D operating at

11

12 $F_{sampling} = 102.4 \text{ MHz.}$

13

14 The extent of oversampling and the specific frequency chosen are in accordance with
15 criteria discussed in the next section below. Subsequent to the digitizer, the
16 oversampled input is selected and scaled as discussed previously above. With
17 reference now made to Fig. 5, the oversampled, selected, scaled, input stream 3050 is
18 subsequently digitally down-converted within baseband conversion 4000 into
19 baseband orthogonal component streams (4150-I and 4150-Q). This is done by
20 parallel multiplications 4100-I and 4100-Q of the digitized signal 3050 with the
21 quadrature local oscillator signals 4125-I and 4125-Q, represented by the complex
22 exponential

23

24 $e^{2j\pi k F_i T_{sampling}}$

25

26 where F_i is the nominal carrier frequency and

1

2

$$T_{sampling} = 1/F_{sampling}$$

3

4 Each of the quadrature baseband digital streams (4150-I and 4150-Q) is then parallel
5 processed by the Filtering and Decimation functions 5000 in respective but otherwise
6 identically implemented filter and decimation pipelines. For each pipeline, 2 low-
7 pass FIR (finite impulse response) filters (5100 and 5300), 2 decimators (5200 and
8 5400), and a matched filter 5600 are provided. The number and arrangement of the
9 filters and decimators are chosen for reasons discussed in the next section below.
10 However, the overall purpose of the decimators is to reduce the number of samples to
11 a constant 4 samples per symbol period, independent of baud rate.

12

13 The purpose of the low-pass filters is to reject the image frequencies resulting from
14 the baseband conversion and any adjacent undesired carriers. In the illustrated
15 preferred embodiment, each low-pass filter is implemented as a cascaded integrator
16 comb (CIC) filter. The impulse response of the CIC filter is given by

17

18
$$\left(\sum_{i=0}^N z^{-i} \right)^D,$$

19

20 where N corresponds to the decimation factor and D to the number of cascaded
21 integrators. With $D=4$, better than 50dB of out-of-band rejection is obtained, which is
22 sufficient for the applications of the illustrated embodiments.

23

24 In a purely theoretical receiver, the matched filter of the front-end should have an
25 impulse response exactly matched to that of the theoretical transmit filter. Both may

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1 be chosen to be identical square-root raised-cosine filters, so that their cascade
2 provides a raised cosine Nyquist filter. Such a filter guarantees zero-ISI (zero-
3 intersymbol interference) while minimizing the noise at the detector input. In actual
4 implementations, the CIC filters have a known non-ideal response (it is not flat) in the
5 pass band that can be compensated for by appropriate adjustments to the response of
6 the matched filter. Thus in the illustrated preferred embodiment, the matched filter
7 implements an FIR whose coefficients are those of a squared-root raised cosine filter
8 compensated for the CIC filters attenuation.

9

10 Multi-Symbol Rate Demodulation Using a Fixed Sampling Rate

11 In an illustrative embodiment compatible with the DOCSIS standard, the sampling
12 frequency is chosen to be a fixed integer multiple of all symbol rates in accordance
13 with another aspect of the present invention. Recall that in the DOCSIS standard,
14 each of the input coax cables may have a multiplex of carriers located in the 5-42
15 MHz range and that each carrier may have any symbol rate from 5 possible values
16 (160 kBaud, 320 kBaud, 640 kBaud, 1280 kBaud, 2560 kBaud).

17

18 In particular, the sampling frequency is chosen to be an integer multiple of 4 times the
19 symbol rates, so that 4 samples per symbol interval can be fed to the matched filter
20 after simple decimation. Furthermore, since the multiplex on each cable has a
21 spectrum which spans the 5-42 MHz frequency range, the sampling frequency must
22 be higher than 84 MHz (twice the maximum frequency). All these conditions are
23 satisfied by the previously cited sampling frequency of 102.4 MHz. This frequency
24 corresponds to an over-sampling factor equal to 10, 20, 40, 80, 160 when the baud
25 rate is 2560 kBaud, 1280 kBaud, 640 kBaud, 320 kBaud, 160 kBaud, respectively.

26

1 A number of options are possible in implementing the tuner's decimation from the
2 A/D sample rate to the 4 samples per symbol interval rate. For the illustrative
3 application, the tuner decimates by a selected total factor of 10, 20, 40, 80, or 160. It
4 is possible to achieve these rate changes in a single stage with a configurable
5 decimation (rate change) factor, through multiple stages of which each has a
6 configurable decimation factor, or through multiple stages of which some have a fixed
7 decimation factor and others have a configurable decimation factor. In multiple stage
8 decimation approaches, the particular rate change stage partitioning (or ordering) used
9 to accomplish the total required rate change is not crucial to the overall operation.
10 While a particular partitioning and ordering is used in the illustrative embodiment,
11 practitioners will realize that other partitioning and orderings are possible within the
12 scope of the present invention.

13

14 In the embodiment illustrated in both Fig. 2 and Fig. 5, the tuner is partitioned into
15 multiple sample-frequency clock domains. The first domain 1100 operates at the
16 fixed A/D sample rate and includes in common the A/Ds 930 of the N digitizers 900,
17 the baseband converters 4100, and the first decimators 5200 of the M front-ends 6000.
18 Additional clock domains 1300 exist, including a plurality operating at selectable sub-
19 multiples of the first domain (or second domain, if any, as discussed below) as
20 required to deliver a constant number of symbol samples (4 in the illustrated
21 embodiment) to each matched filter of the respective front-ends.

22

23 In an optional but preferred embodiment, a second domain 1200, including a second
24 decimator 5400, operates at a fixed sub-multiple of the first domain. Using this
25 preferred approach, the decimation is done in two separate steps. The first decimator
26 5200 operates with a constant "rate change" ratio equal to 10 (i.e., it keeps one of

1 every 10 samples). The second decimator 5400 has a configurable rate change ratio
2 whose value is selectable between 1 and 16, depending on the symbol rate. The
3 dependence of the rate change ratio on the symbol rate as it is shown in Table 1.

4

5 **Table 1. Rate Change Ratio for each Symbol Rate.**

Symbol rate (kBaud)	Total rate change ratio	1 st stage rate change ratio	2 nd stage rate change ratio
160	160	10	16
320	80	10	8
640	40	10	4
1280	20	10	2
2560	10	10	1

6

7

8 In summary, in the illustrated embodiment only the first stages of the front-end
9 operate at the sampling frequency of 102.4 MHz, while subsequent stages operate at
10 10.24 MHz, and the final stages (including the matched filter) operate at 4 times the
11 symbol rate.

12

13 The clocking approach taught by the present invention enables producing matched
14 front-end outputs using only simple filters and decimation, eliminates the need for
15 interpolation stages, maximizes commonality of function, and provides reduced
16 complexity and costs over previous approaches.

17

18

1 System-Level Implementation

2 Fig. 6 illustrates preferred chip-boundary partitions for two different illustrative
3 embodiments of the tuner 1000 of Fig. 2. It is desirable to implement as much as
4 possible of the tuner 1000 on a single integrated circuit, consistent with sound
5 engineering and business practice. System partition 1050 corresponds to a preferred
6 illustrative implementation, wherein all stages of the tuner following variable gain
7 amplifier 920 are integrated on a single integrated circuit, generally with other
8 functions. However, due to the size and complexity of the A/Ds, the more
9 conservative system partition 1050 may be chosen.

10

11 Figs. 7 and 8A-C further illustrate an exemplary system-level application of the
12 present invention. Fig. 7 illustrates a mini-Fiber-Node/mini-Cable-Modem-
13 Termination-System (mFN/mini-CMTS) 8000. The mini-CMTS 9000 implements a
14 multi-channel digital receiver that employs a tuner 1000 in accordance with the
15 present invention. Consistent with the system partition 1050 of Fig. 6., the front-end
16 portion 6000 of the tuner is implemented on the DSP multi-channel transceiver ASIC
17 7000. Also implemented on the ASIC is the multi-channel demodulator portion of the
18 digital receiver as well as the all-digital portions of a multi-channel digital transmitter.
19 The tuner 1000 accepts multiple coax inputs 1800, delivers digitized equivalent
20 streams 1700 from the output of digitizer portion 900, and delivers baseband
21 converted and isolated quadrature digitized signals 1900, suitable for demodulation.
22 The realization locally within the mFN of the CMTS functions, in general and the
23 demodulator functions in particular, is made practical for widespread deployment by
24 the teachings of the present invention.

25

1 Fig. 8A shows the relationship between the mFN and subscribers (indicated by homes
2 having Customer Premise Equipment, CPE) and between the mFN and the cable
3 system head end 10100. Each mFN is coupled to up to 50 to 70 homes (50-70
4 Households Passed, HHP). Each mFN is coupled to the head end via a regional
5 packet network 10150. This packet network is usually implemented as a packet fiber
6 overlay for a downstream legacy analog HFC distribution. Fig. 8B provides detail of
7 the CPE, which generally includes a television, the cable "set-top" box, and a cable
8 modem for coupling the subscriber's personal computer to the network. In some
9 systems, the CPE may additionally include an interface to a subscriber telephone.

10

11 Fig. 8C shows the Head End 10100 as a component within the Internet 10000. As
12 indicated in the legend, many subcomponents are part of this network. In this
13 conceptual drawing, multiple backbone networks 10050-1 through 10050-N,
14 generally operated by different long-haul communications companies, are
15 interconnected via Peering Point 10100-1 (and other peering points not shown). Dial-
16 up access provider 10500, Server Farm 10400, corporate network 10300, and cable
17 system head end 10100, contract for access to the various backbone networks.
18 Corporate end-user 10390 has network access via the associated corporate network
19 10300. Private end-user 10550 has access via dial-up connection 10540. Thus in the
20 illustrated embodiments provided, cable subscribers (as indicated by homes illustrated
21 in Fig. 8A) provide or gain access to content, services, e-mail, and other Internet
22 resources, via a path that includes the multiple input, multiple channel output, digital
23 tuner of the present invention.

24

25

26

1

Conclusion

2

3 Although the present invention has been described using particular illustrative
4 embodiments, it will be understood that many variations in construction, arrangement
5 and use are possible consistent with the teachings and within the scope of the
6 invention. For example, bit-widths, clock speeds, and the type of technology used
7 may generally be varied in each component block of the invention. Also, unless
8 specifically stated to the contrary, the value ranges specified, the maximum and
9 minimum values used, are merely those of the illustrative or preferred embodiments
10 and should not be construed as limitations of the invention. Specifically, other
11 embodiments may use different clock multiples or sub-multiples, different frequency
12 bands, different modulation schemes, and different numbers of inputs and output
13 channels. Functionally equivalent techniques known to those skilled in the art may
14 be employed instead of those illustrated to implement various components or sub-
15 systems. For example, the selector and scaler functions may be implemented using
16 pass-gates or tri-state buffers and not just via the preferred AND-OR gating. All such
17 variations in design comprise insubstantial changes over the teachings conveyed by
18 the illustrative embodiments. The names given to interconnect and logic are
19 illustrative, and should not be construed as limiting the invention. It is also
20 understood that the invention has broad applicability to other communications and
21 network applications, and is not limited to the particular application or industry of the
22 illustrated embodiments. The present invention is thus to be construed as including
23 all possible modifications and variations encompassed within the scope of the
24 appended claims.

25

26

1 What is claimed is:

2

3 1) A method of operating a digital tuner, comprising:

4 digitizing a first number of input signals to create respective streams of
5 digitized input data;

6 providing a second number of per-channel front-ends for performing baseband
7 translation and filtering in the digital domain and providing outputs
8 suitable for subsequent demodulation;

9 providing each per-channel front-end with an input selector coupled to each of
10 the streams of digitized input data; and

11 configuring each of the per-channel front-ends to process a selected one of the
12 first number of streams of digitized input data.

13

14

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1 2. A method of operating a digital tuner, comprising:

2 providing a first number of A/D converters for digitizing a first number of

3 input signals to create respective streams of digitized input data;

4 providing each A/D converter with a preceding variable-gain amplifier;

5 setting the amplifier gain as a function of the entire carrier multiplex present

6 on the input signals;

7 providing a second number of per-channel front-ends for performing baseband

8 translation and filtering in the digital domain and providing outputs

9 suitable for subsequent demodulation;

10 providing each per-channel front-end with a respective digital signal scaler

11 coupled to a selected one of the streams of digitized input data;

12 providing the output of the scaler to the subsequent stages of its respective

13 per-channel front-end; and

14 for each per-channel front-end, dynamically scaling the selected incoming

15 stream of digitized input data as a function of the signal power of the

16 desired carrier to minimize variations in the peak magnitude of the

17 signals processed.

18

19

1 3. A method of operating a digital tuner, comprising:
2 providing a first plurality of input signals having a second plurality of symbol
3 rates;
4 providing a first sampling clock that is a common integer multiple of the
5 second plurality of symbol rates;
6 digitizing the first plurality of input signals using the first sampling clock to
7 create respective streams of digitized input data;
8 providing a third plurality of per-channel front-ends, each front-end having a
9 baseband converter, a first decimator, and a matched filter;
10 operating the baseband converter and the first decimator of each per-channel
11 front-end at the first sampling clock; and
12 for each per-channel front end, providing a selectively decimated number of
13 samples to each matched filter and operating each matched filter at a
14 selected compatible sampling clock, such that a constant number of
15 symbol samples is output from each matched filter.

16

1 4. A digital tuner, comprising:

2 a first plurality of digitizers operating at a common first sampling rate and
3 providing a first plurality of digitized data streams corresponding to a
4 first plurality of analog inputs;

5 a second plurality of digital front-ends, each front-end including
6 selector circuitry for selectable coupling of one of the first plurality of
7 digitized data streams to post-selector processing circuitry of
8 the associated front-end, each selector operating independently
9 of the other selectors,

10 digital frequency conversion circuitry having a selectable conversion
11 frequency from a predetermined set of conversion frequencies,
12 and

13 post-conversion circuitry having a selectable decimation factor from a
14 predetermined set of decimation factors, the post-conversion
15 circuitry providing an output suitable for subsequent processing
16 by a digital demodulator; and

17 wherein configuration of the tuner may select any arbitrary combination of
18 one of the first plurality of analog inputs, one of the set of conversion
19 frequencies, and one of the set of decimation factors.

20

21 5. The digital tuner of claim 4, wherein the configuration of the tuner is
22 accomplished programmatically.

23

24 6. The digital tuner of claim 4, wherein the configuration of the tuner is
25 accomplished remotely.

1 7. The digital tuner of claim 4, wherein the configuration of the tuner is
2 accomplished automatically.

3

4 8. The digital tuner of claim 4, wherein the configuration of the tuner is
5 accomplished dynamically.

6

7 9. The digital tuner of claim 4, wherein the configuration of the tuner is
8 accomplished without involving a human operator.

9

10 10. The digital tuner of claim 4, wherein the common first sampling rate is an integer
11 multiple of each decimation factor of the predetermined set of decimation
12 factors.

13

14 11. The digital tuner of claim 4, wherein each decimation factor of the predetermined
15 set of decimation factors is an integer sub-multiple of the common first
16 sampling rate.

17

18 12. The digital tuner of claim 4, wherein the post-conversion circuitry is implemented
19 as a single stage having a configurable decimation factor selected from a
20 predetermined set.

21

22 13. The digital tuner of claim 12, wherein the predetermined set includes decimation
23 factors of 10, 20, 40, 80, and 160.

24

25

1 14. The digital tuner of claim 4, wherein the post-conversion circuitry is implemented
2 as multiple stages of which some have a fixed decimation factor and others
3 have a configurable decimation factor.

4

5 15. The digital tuner of claim 14, wherein the post-conversion circuitry is
6 implemented using a first stage having a fixed decimation factor and a second
7 stage having a configurable decimation factor selected from a predetermined
8 set.

9

10 16. The digital tuner of claim 15, wherein the fixed decimation factor is 10.

11

12 17. The digital tuner of claim 15, wherein the predetermined set includes decimation
13 factors of 1, 2, 4, 8, and 16.

14

15 18. The digital tuner of claim 15, wherein the fixed decimation factor is 10 and the
16 predetermined set includes decimation factors of 1, 2, 4, 8, and 16.

17

18 19. The digital tuner of claim 4, wherein the post-conversion circuitry is implemented
19 as multiple stages of which each has a configurable decimation factor.

20

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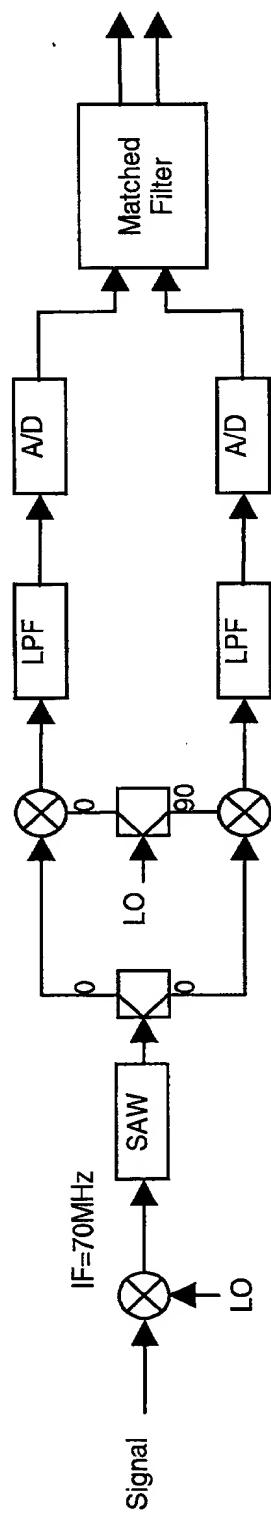
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ABSTRACT

2

3 The present invention teaches a compact and highly integrated multiple-channel
4 digital tuner and receiver architecture, suitable for widespread field deployment,
5 wherein each receiver demodulator channel may be remotely, automatically,
6 dynamically, and economically configured for a particular cable, carrier frequency,
7 and signaling baud-rate, from an option universe that includes a plurality of input
8 cables, a plurality of carrier frequencies, and a plurality of available baud-rates. A
9 multiple coax input, multiple channel output, digital tuner is partitioned into a
10 multiple coax input digitizer portion and a multiple channel output front-end portion.
11 The digitizer portion consists of N digitizers and accepts input signals from N coax
12 cables and digitizes them with respective A/D converters. The front-end portion
13 consists of M front-ends and provides M channel outputs suitable for subsequent
14 processing by M respective digital demodulators. In a first clock domain, a fixed
15 predetermined A/D sampling rate is chosen to provide oversampling of the inputs by a
16 common integer multiple of all the symbol rates of interest. A plurality other clock
17 domains operate at selectable sub-multiples of the first domain as required to deliver a
18 constant number of symbol samples at the output of each front-end. At the input to
19 each of the M front-ends is a respective input selector coupled to each of the N
20 streams of digitized input data followed by a digital signal scaler that dynamically
21 scales the selected incoming stream of digitized input data as a function of the signal
22 power of the channel's associated carrier.

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Prior Art
Fig. 1

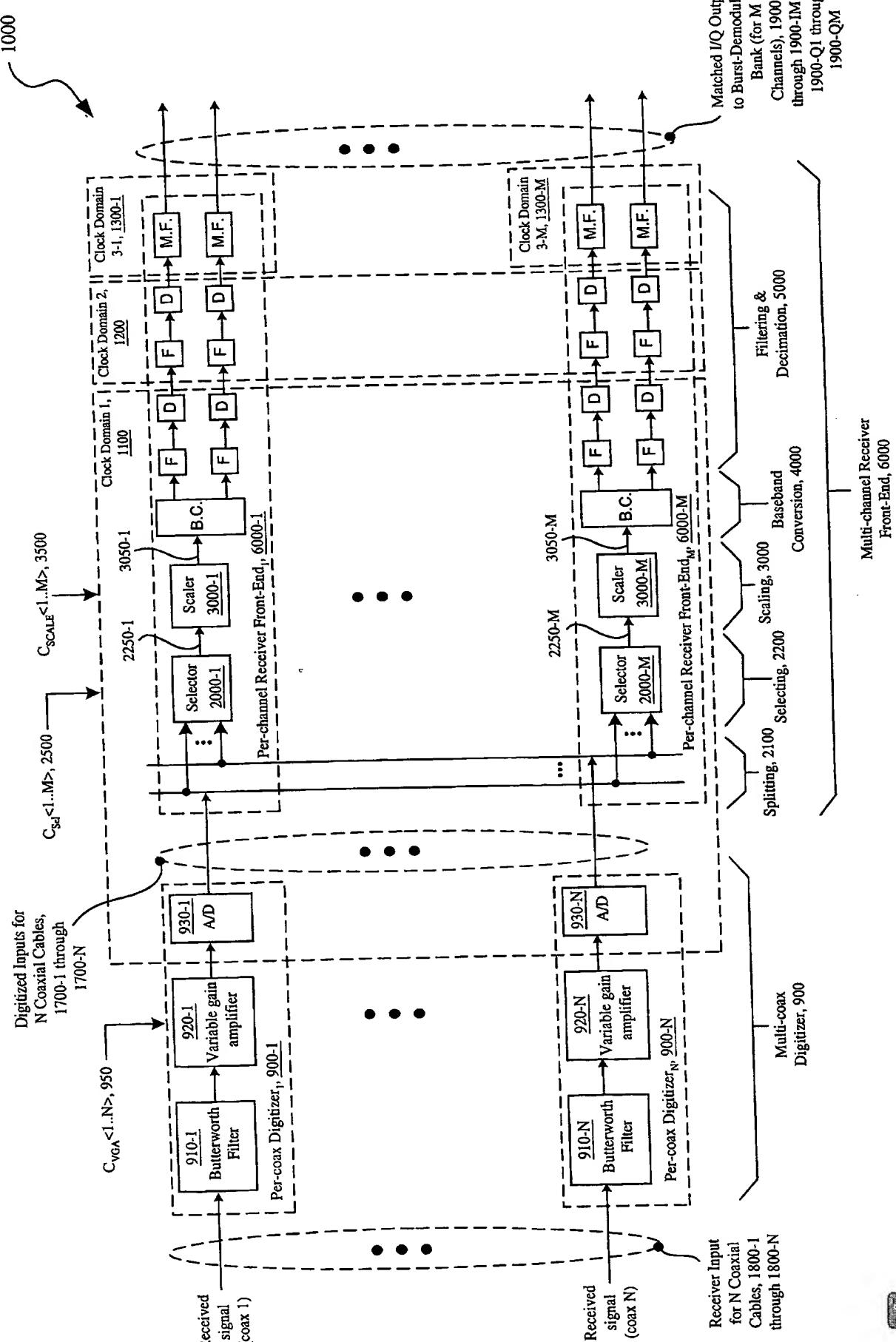


Fig. 2

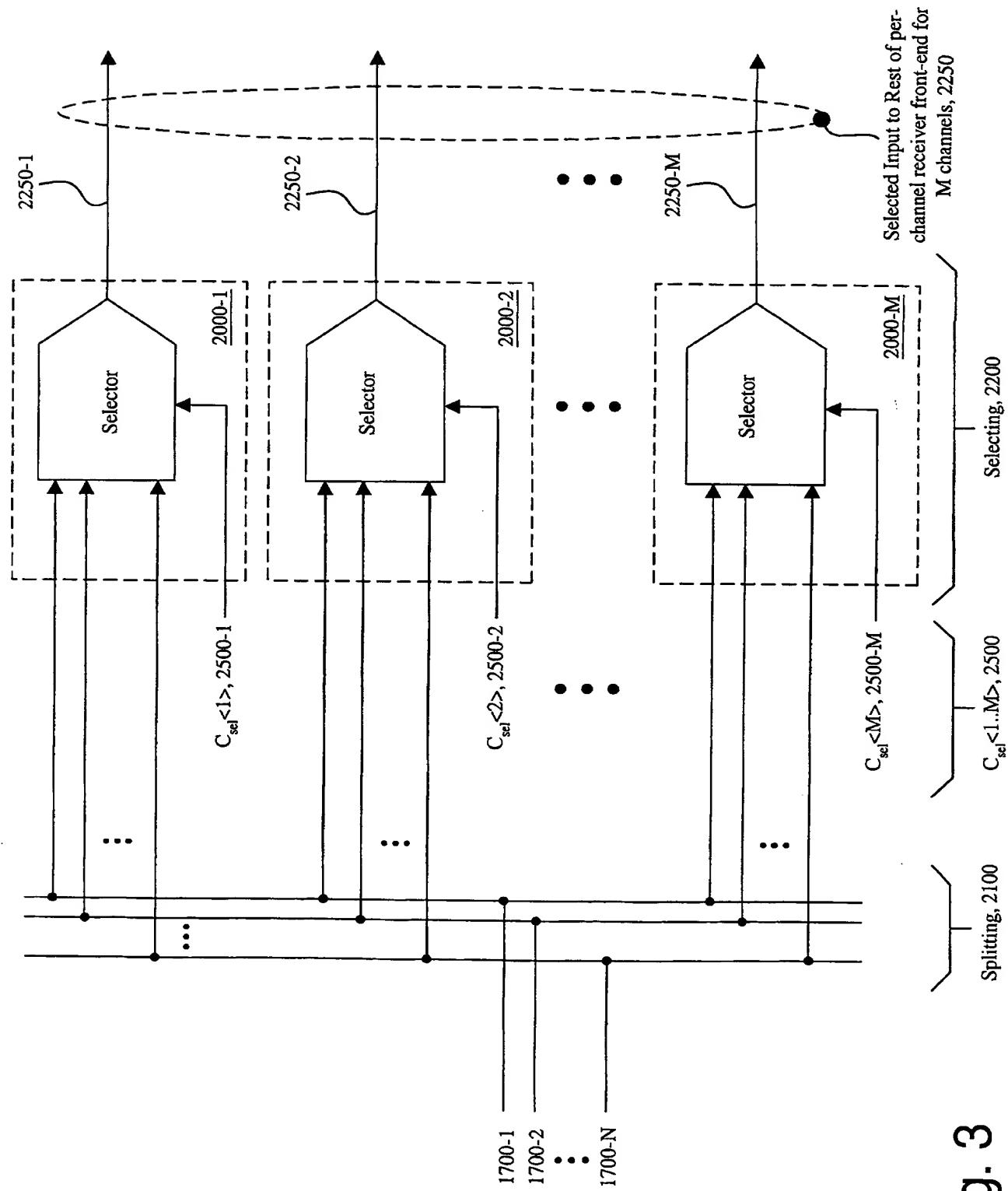


Fig. 3

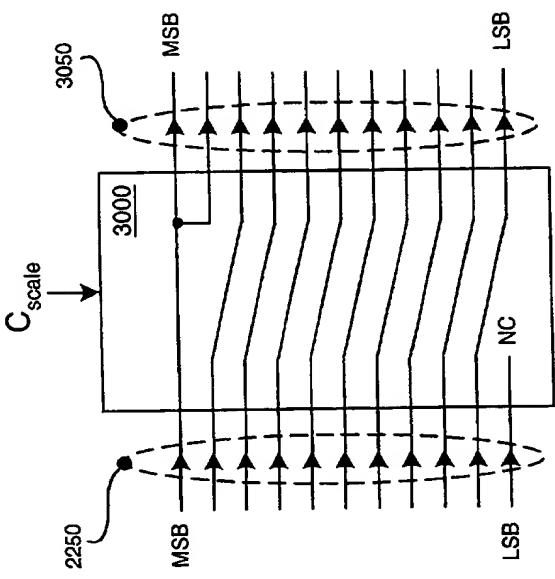
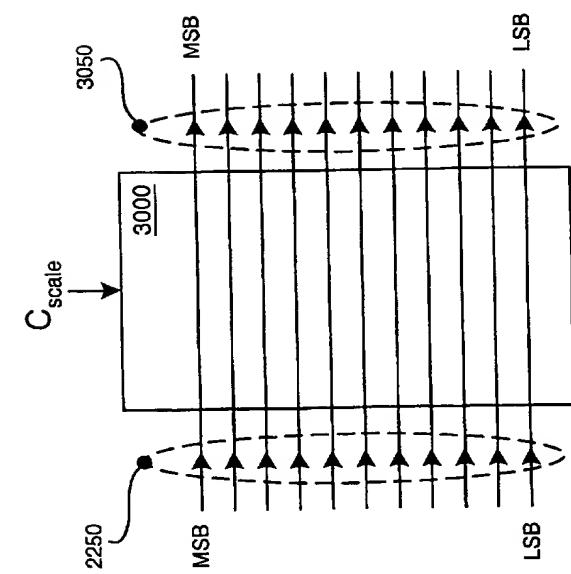
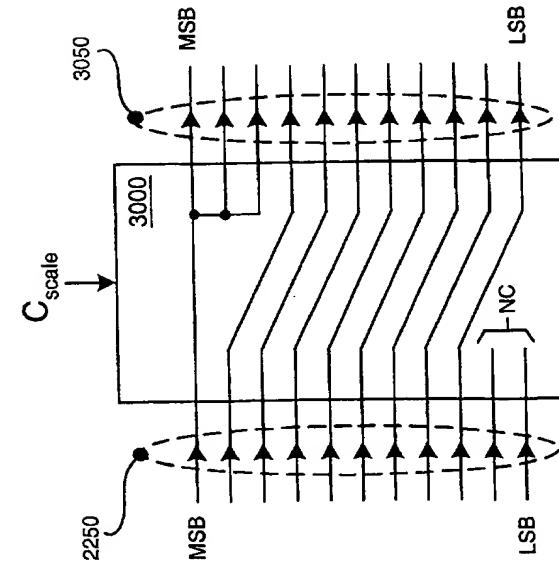
DIVIDE BY 2 (Shift by one bit in LSB Direction)
(A)DIVIDE BY 2 (Shift by one bit in LSB Direction)
(B)DIVIDE BY 4 (Shift by two bits in LSB Direction)
(C)

Fig. 4

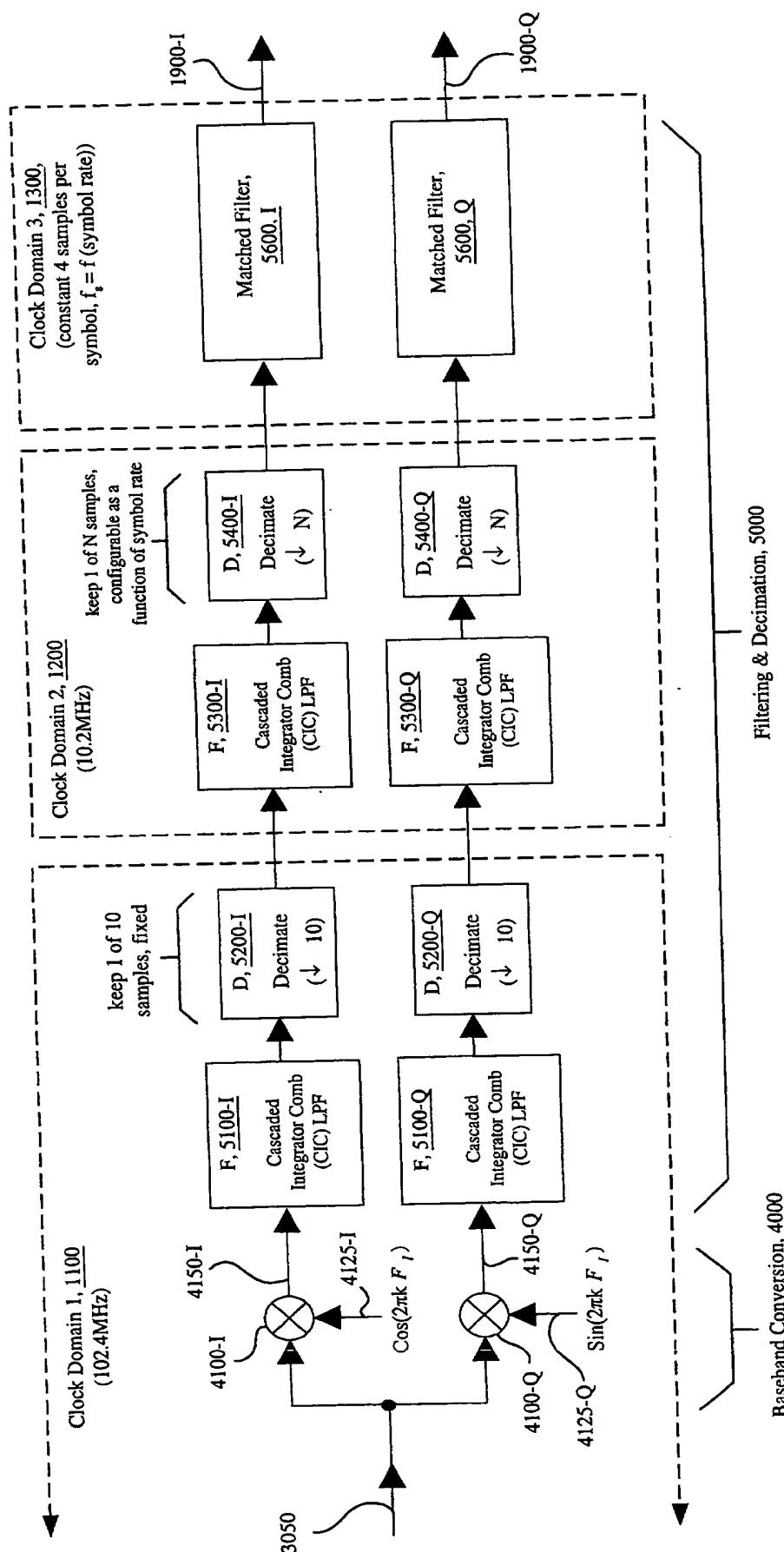
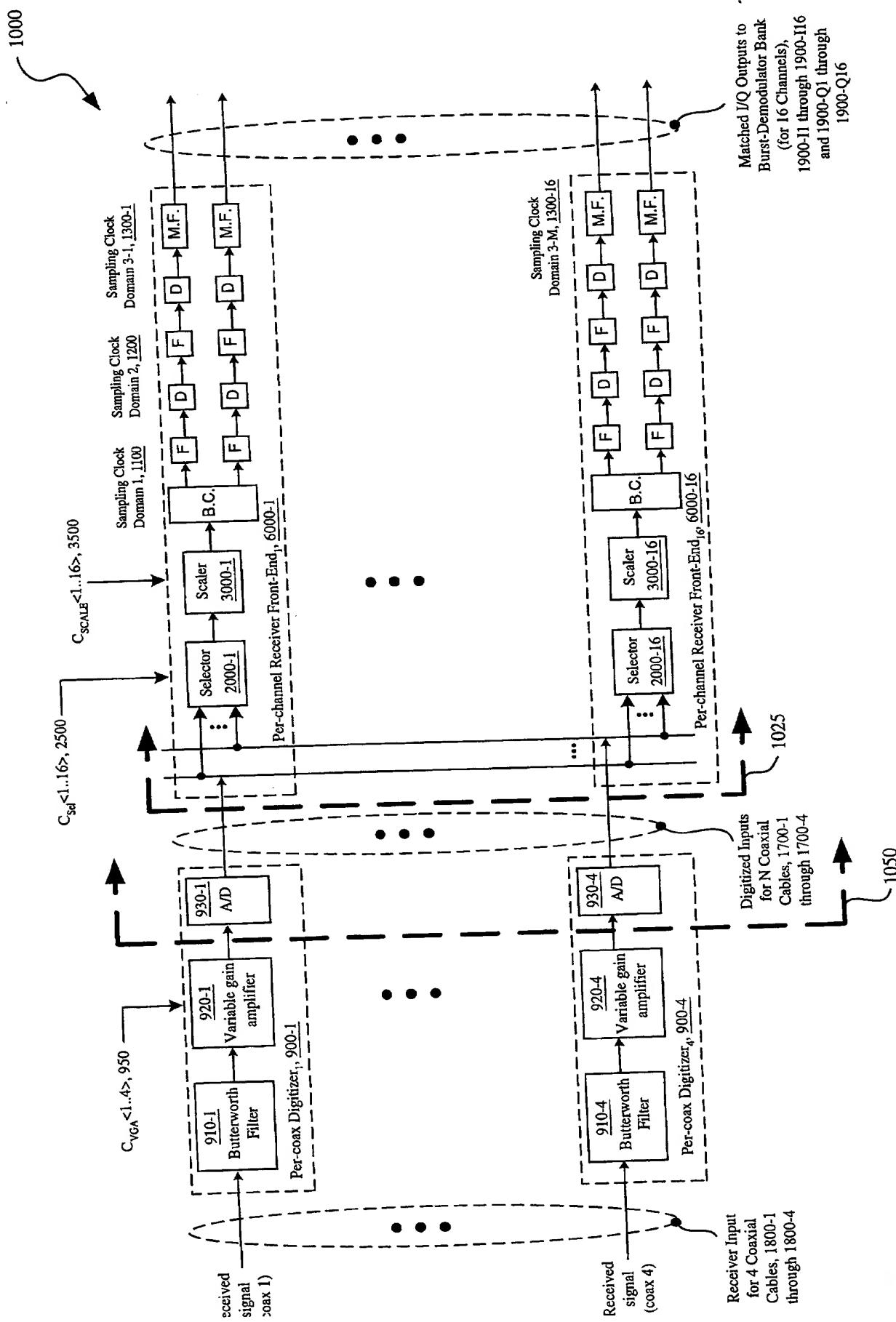


Fig. 5



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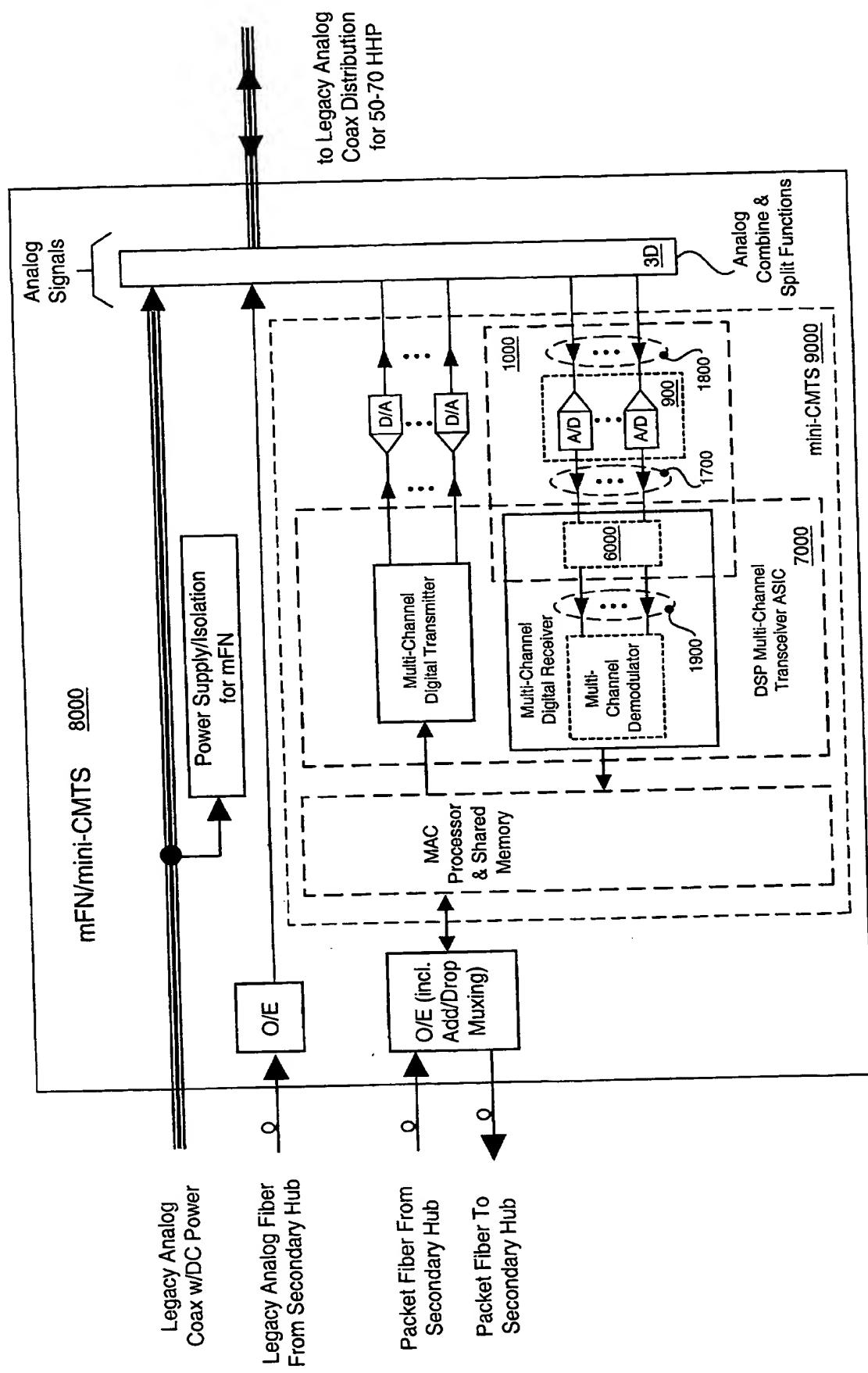


Fig. 7

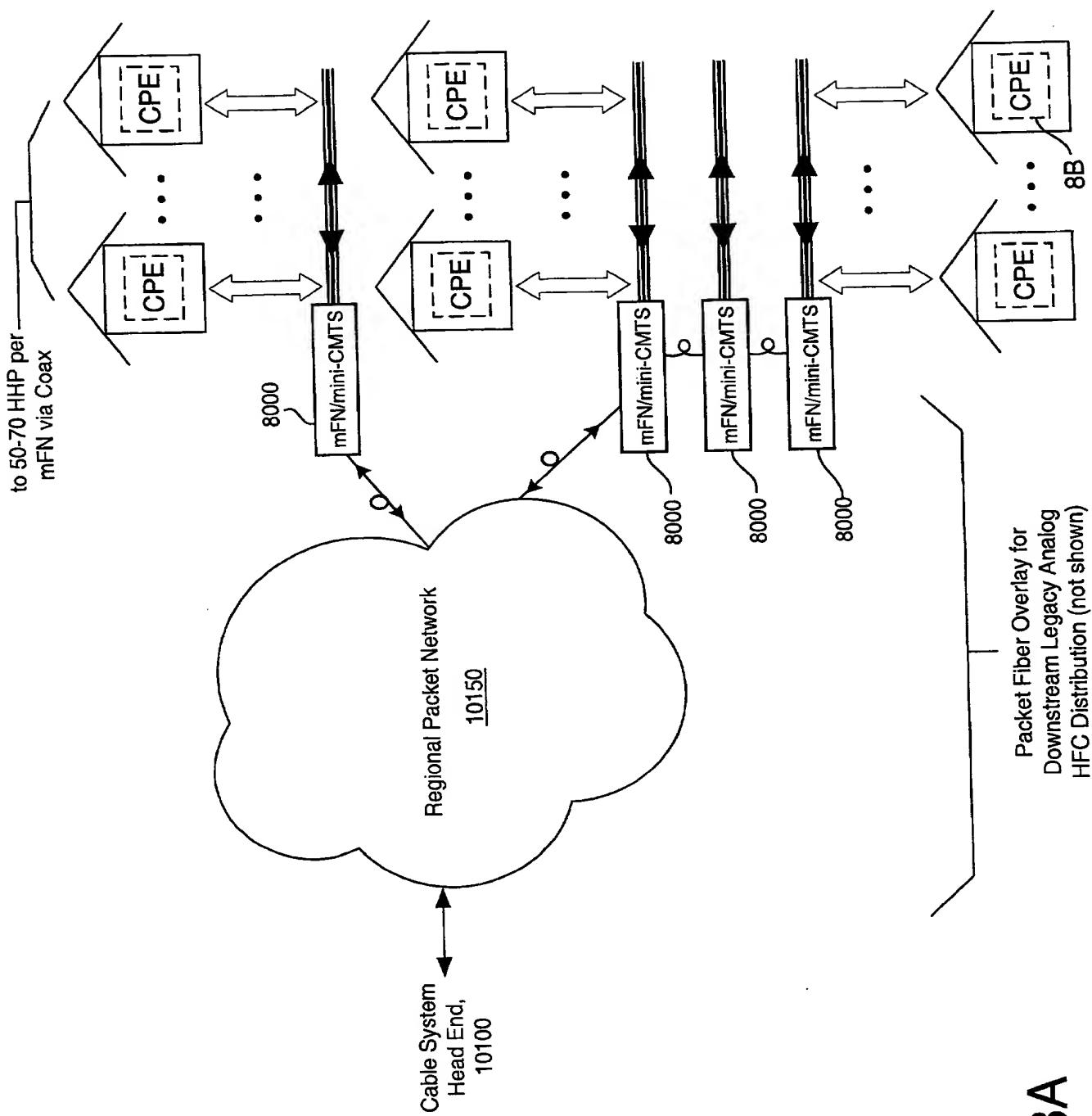
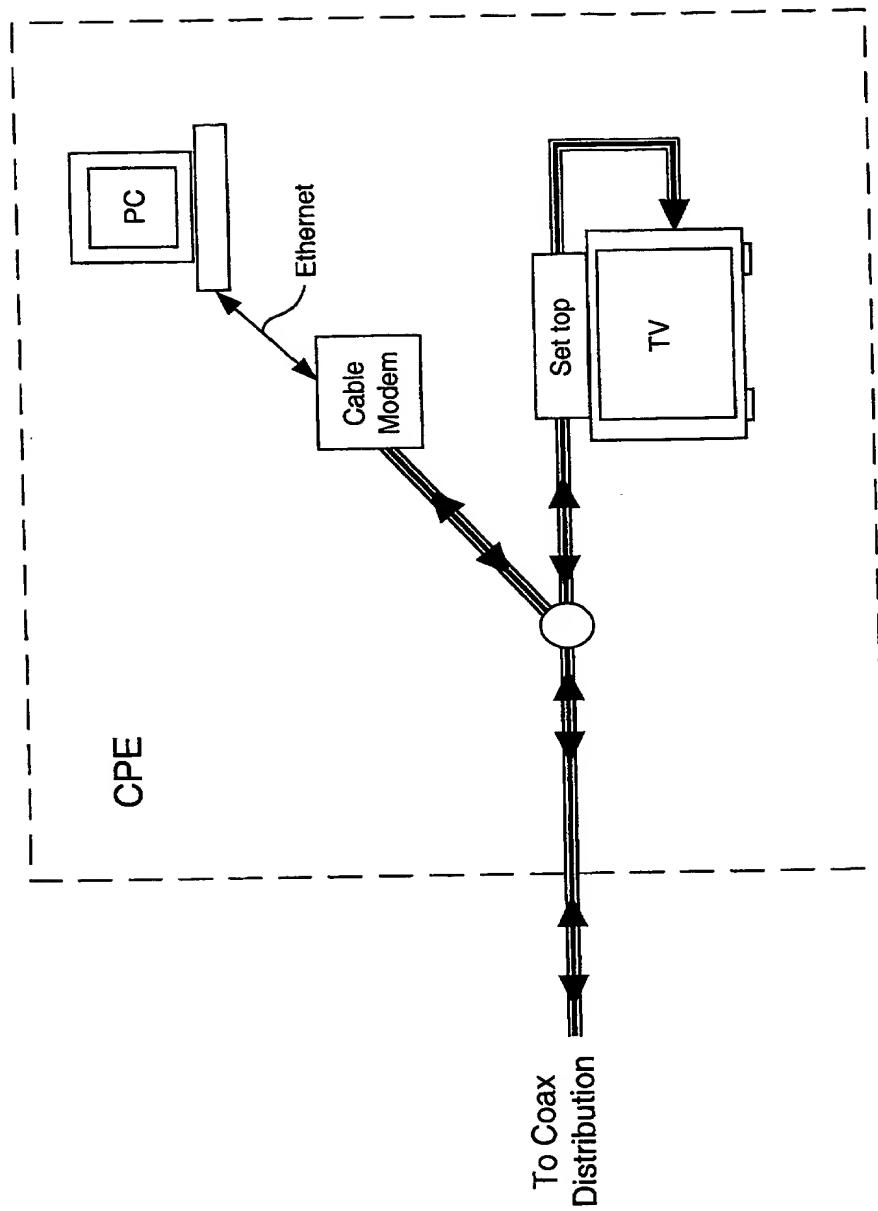


Fig. 8A



Prior Art
Fig. 8B

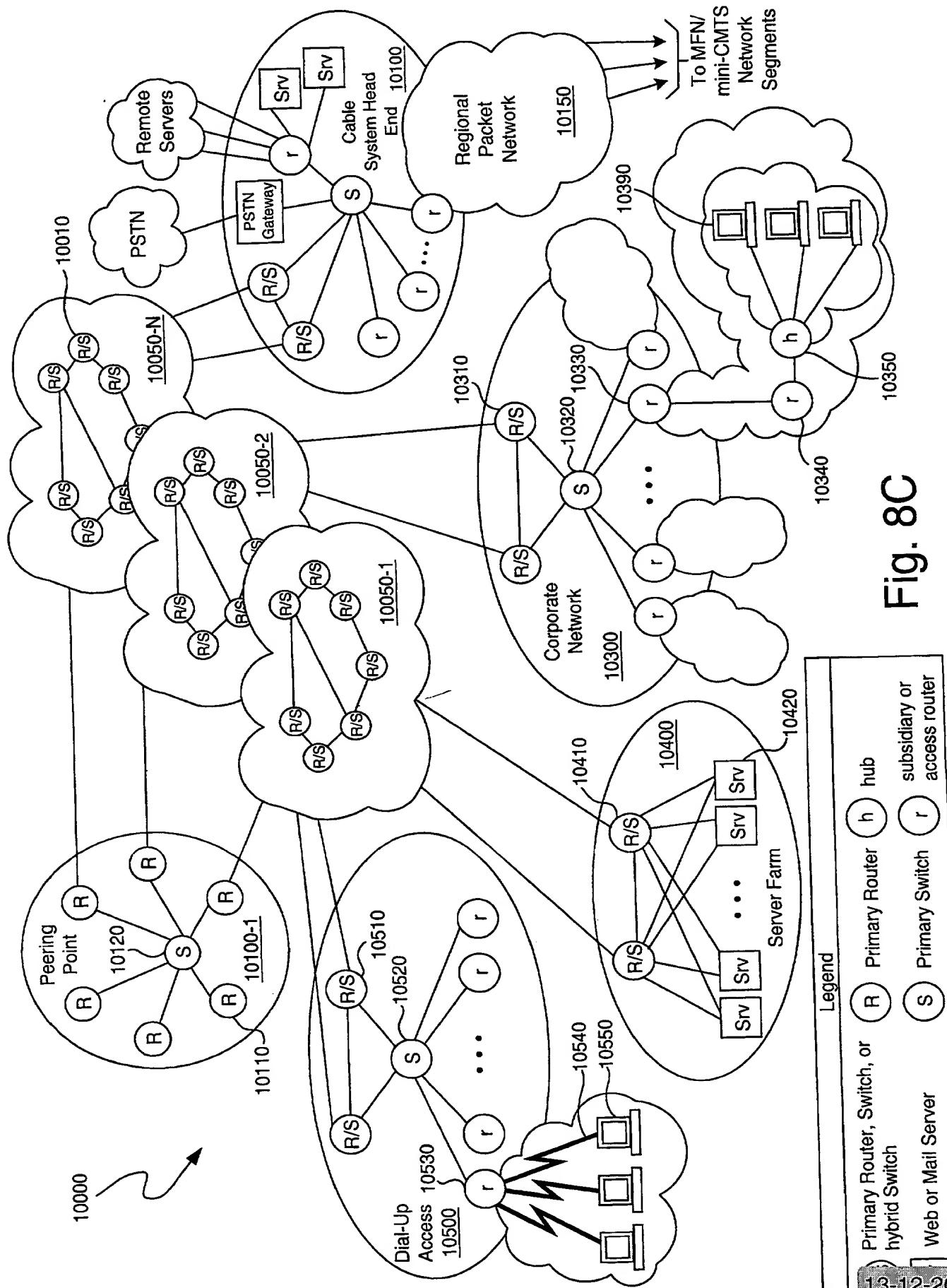


Fig. 8C